This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-55 (Cancelled)

Claim 56 (Currently Amended) A planar hybrid-orientation semiconductor substrate structure comprising:

at least one clearly defined first single crystal semiconductor region having a first surface crystal orientation, and

at least one clearly defined second single crystal semiconductor region having a second surface crystal orientation different from the first, said second single crystal semiconductor region is formed by amorphizing a semiconductor material having said first orientation and recrystallizing it into a semiconductor material having said second orientation, and said first single crystal semiconductor region ~~and~~ is laterally adjacent to said second single crystal semiconductor region and ~~are~~ both regions are disposed directly on a common buried insulating layer that lays atop a substrate.

Claim 57 (Previously Presented) The planar hybrid-orientation substrate structure of Claim 56 further comprising at least one isolation region separating said at least one first single crystal semiconductor region from said at least one second single crystal semiconductor region.

Claim 58 (Cancelled)

Claim 59 (Previously Presented) The planar hybrid-orientation substrate structure of Claim 57 wherein said at least one isolation region comprises a dielectric-filled trench.

Claim 60 (Previously Presented) The planar hybrid-orientation substrate structure of Claim 56 wherein materials of said first and second semiconductor regions are selected from the group

consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

Claim 61 (Previously Presented) The planar hybrid-orientation substrate structure of Claim 56 wherein said clearly defined first and second single crystal semiconductor regions with different surface orientations both comprise a Si-containing semiconductor material.

Claim 62 (Previously Presented) The planar hybrid-orientation substrate structure of Claim 56 wherein said at least two clearly defined single crystal semiconductor regions are each comprised of strained, unstrained or a combination of strained and unstrained semiconductor materials.

Claim 63 (Previously Presented) The planar hybrid-orientation substrate structure of Claim 61 wherein said different surface crystal orientations are selected from the group consisting of (110), (111) and (100).

Claim 64 (Previously Presented) The planar hybrid-orientation substrate structure of Claim 61 wherein said first Si-containing semiconductor region has a (100) crystal orientation and said second Si-containing semiconductor region has a (110) crystal orientation.

Claim 65 (Previously Presented) The planar hybrid-orientation substrate structure of Claim 61 wherein one of said semiconductor regions has a (110) crystal orientation and said other semiconductor region has a (100) crystal orientation.

Claim 66 (Previously Presented) The planar hybrid-orientation substrate structure of Claim 56 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a (100) crystal orientation and said at least pFET device is located on a (110) crystal orientation.

Claim 67 (Previously Presented) The planar hybrid-orientation substrate structure of Claim 56 further comprising at least one nFET device and at least one pFET device, wherein said at least

one nFET device is located on a crystal orientation that is optimal for said nFET device and wherein said at least pFET device is located on a crystal orientation that is optimal for said pFET device.

Claim 68 (Currently Amended) The structure of Claim [[58]] 56 wherein said buried insulator layer is a dielectric material selected from the group consisting of SiO_2, SiO_2 containing nitrogen, silicon nitride, metal oxides, metal nitrides, and highly thermally conductive materials.

Claim 69 (Currently Amended) A planar hybrid-orientation semiconductor-on-insulator (SOI) substrate structure comprising:

at least one single-layer semiconductor region comprising a semiconductor having a first single-crystal surface orientation, and

at least one bilayer semiconductor region comprising a lower semiconductor layer having said first single-crystal surface orientation and an upper semiconductor layer having a second single-crystal surface orientation different from the first, wherein said at least one single-layer semiconductor region ~~and~~ is laterally adjacent to said at least one bilayer semiconductor region ~~are~~ and both regions are disposed directly on a common buried insulating layer, said insulating layer is located on a substrate.

Claim 70 (Previously Presented) The structure of Claim 69 further including at least one isolation region separating said at least one single-layer semiconductor region from said at least one bilayer semiconductor region.

Claim 71 (Previously Presented) The structure of Claim 69 wherein said isolation region extends down at least to said common buried insulating layer.

Claim 72 (Previously Presented) The structure of Claim 69 wherein said common buried insulator layer is a dielectric material selected from the group consisting of SiO_2, SiO_2 containing nitrogen, silicon nitride, metal oxides, metal nitrides, and highly thermally conductive materials.

Claim 73 (Previously Presented) The planar hybrid-orientation substrate structure of Claim 69 wherein said single-layer and bilayer semiconductor regions both comprise a semiconductor material selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

Claim 74 (Previously Presented) The structure of Claim 69 wherein said single-layer and bilayer semiconductor regions both comprise a Si-containing semiconductor material.

Claim 75 (Previously Presented) The structure of Claim 69 wherein said single-layer and bilayer semiconductor regions are each comprised of strained, unstrained or a combination of strained and unstrained semiconductor materials.

Claim 76 (Previously Presented) The planar-hybrid-orientation SOI substrate structure of Claim 69 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said nFET device and wherein said at least pFET device is located on a crystal orientation that is optimal for said pFETdevice.

Claim 77 (Previously Presented) The planar hybrid-orientation SOI substrate structure of Claim 69 wherein said different surface orientations are selected from the group consisting of (110), (111) and (100).

Claim 78 (Previously Presented) The planar hybrid-orientation SOI substrate structure of Claim 69 wherein one of said semiconductor regions has a (100) crystal orientation and said other semiconductor region has a (110) crystal orientation.

Claim 79 (Previously Presented) The planar hybrid-orientation SOI substrate structure of Claim 69 further comprising at least one nFET device and at least one pFET device, wherein said at

least one nFET device is located on a (100) crystal orientation and said at least pFET device is located on a (110) crystal orientation.

Claim 80 (Cancelled)